This listing of claims will replace all prior versions, and listings, of claims in the present application:

Listing of Claims:

Claims 1-9 (previously cancelled).

Claim 10 (amended) An integrated circuit, comprising:

a plurality of logic gates for implementing a logic function of the integrated circuit; and

a self-test circuit for performing an internal self test of the plurality of logic gates, the self-test circuit including a test pattern generator for generating a test pattern, a test response analyzer for evaluating a test response, and an input/output circuit via which the self-test circuit further performs a logic test of an external circuit, the self-test circuit testing both the plurality of logic gates and the external circuit at the same time, wherein a first part of the test pattern is supplied to the plurality of logic gates and a second part of the test pattern is supplied to the external circuit via the input/output circuit, and the test response is produced from a first part of the test response from the plurality of logic gates and a second part of the test response from the external logic circuit, the input/output circuit further including controllable input/output drivers for sending and receiving bidirectional signals between the self-test circuit and the external circuit, the self-test circuit further including a control device for controlling the controllable input/output drivers, and the input/output circuit further including a bus connection for connecting to an external bus structure, with the control device including a bus control wherein external circuit elements connected to the bus structure are selectively selected for a self-test via respective enable signals, and the bus control including a counter for counting a bus clock signal, wherein the controllable input/output drivers are only selected during one of all even-numbered clock cycles and all odd-numbered clock cycles of the bus clock signal and the respective enable signals are output sequentially during one of all odd-numbered clock cycles and all even-numbered clock cycles of the bus clock signal, which are not selected for the controllable input/output drivers, for enabling the respective external circuit elements.

Claim 11 (previously presented) An integrated circuit as claimed in claim 10, wherein both the test pattern generator and the test response analyzer are linear-feedback shipped registers.

Claim 12 (previously presented) An integrated circuit as claimed in claim 10, wherein the test pattern generator generates pseudo-random vectors as the test pattern.

Claim 13 (previously presented) An integrated circuit as claimed in claim 10, wherein the input/output circuit includes input/output drivers for sending and receiving unidirectional signals between the self-test circuit and the external circuit.

Claim 14(cancelled).

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Claim 15 (amended) An integrated circuit as claimed in claim ~~14~~10, wherein the control device controls both the self-test circuit and the output circuit such that an initialization of the external circuit is performed in a first test cycle and the self test of the plurality of logic gates and the logic test of the external circuit are performed in a second test cycle.

Claim 16 (cancelled).

Claim 17 (cancelled).

Claim 18 (amended) An integrated circuit as claimed in claim 10, wherein the input/output circuit ~~can be~~ is optionally selectively deactivated.